**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA**
**KAKINADA – 533 003, Andhra Pradesh, India**
**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

| II Year – II Semester | | L | T | P | C |
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| **DIGITAL IC DESIGN LAB** | | | | | |

Note: The students are required to design and draw the internal logical structure of the following Digital Integrated Circuits and to develop VHDL/Verilog HDL Source code, perform simulation using relevant simulator and analyze the obtained simulation results using necessary synthesizer. All the experiments are required to verify and implement the logical operations on the latest FPGA Hardware in the Laboratory.

List of Experiments: (Minimum of Ten Experiments has to be performed)

1. Realization of Logic Gates

2. Design of Full Adderusing 3 modeling systems

3. 3 to 8 Decoder-74138

4. 8 to 3 Encoder (with and without parity)

5. 8x1Multiplexer-74151 and 2x4De-multiplexer-74155

6. 4-Bit comparator-7485

7. D Flip-Flop-7474

8. Decade counter -7490

9. Shift registers-7495

10. 8-bit serialin-parallel out and parallel in-serial out

11. Fast In & Fast Out (FIFO)

12. MAC (Multiplier &Accumulator)

13. ALU Design.